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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **TAKADA, Kazuhiko**

Group Art Unit: **2811**

Serial No.: **09/528,296**

Examiner: **NADAV, Ori**

Filed: **March 17, 2000**

P.T.O. Confirmation No.: 4124

For: **SEMICONDUCTOR DEVICE HAVING A GUARD RING**

AMENDMENT UNDER 37 CFR § 1.111

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

June 16, 2003

Sir:

In response to the Office Action dated March 14, 2003, please amend the above-identified application as follows:

IN THE CLAIMS:

Amend claim 1 as follows:

1. (Five Times Amended) A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

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wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane